(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
15 September 2005 (15.09.2005)

PCT

(10) International Publication Number
WO 2005/085978 A3

(51) International Patent Classification:
G06F 11/00 (2006.01)

(21) International Application Number:
PCT/IB2005/050575

(22) International Filing Date:
15 February 2005 (15.02.2005)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
04100789.9 27 February 2004 (27.02.2004) EP

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

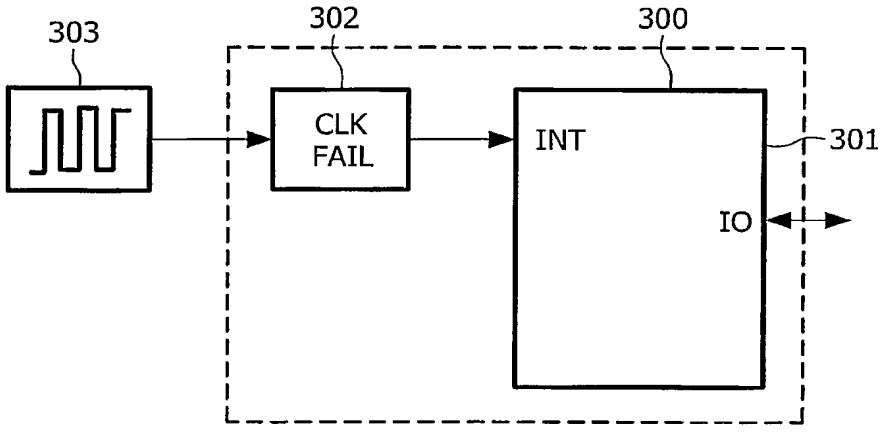
Declaration under Rule 4.17:
— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

Published:
— *with international search report*

(88) Date of publication of the international search report:
18 May 2006

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: ELECTRONIC CIRCUIT ARRANGEMENT FOR DETECTING A FAILING CLOCK



(57) Abstract: The invention relates to an electronic circuit arrangement (300) comprising a clock fail circuit (302) arranged for receiving a clock signal generated by a clock generation circuit (303) and generating an error signal upon the absence of the clock signal. The electronic circuit arrangement (300) further comprises an asynchronous processor (301) arranged for receiving said error signal on an interrupt input INT and to bring the electronic circuit arrangement in a pre-defined state upon detection of the error signal at the interrupt input INT by executing an interrupt routine.

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